



# **PayPass Testing Environment (Terminal Products)**

January 2011

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# Summary of Changes

March 2010:

Table 3.2: The terminal capabilities values must be the same as indicated in the ICS section "4.10 Terminal Data Element Values - Terminal Capabilities".

Table 3.3: '15.00' is the default transaction amount value to be used.

Removed the terminal configuration "PPS\_MStripe3".

Reviewed all the "PPS\_MChipx" terminal configurations.

October 2010:

- CA key Index F1 is used for EVAL tests as well as ETEC tests

The document was aligned with the latest version (2.1) of *PayPass M/Chip Technical Specifications*.

- references to EntryPoint removed

- "Merchant Custom Data" was added to Table 3-2

- added the configuration "PPS\_MC\_Refund"

January 2011:

In the previous document version, the Refund was wrongly introduced as a configuration whereas it should be a transaction type available without the need of re-configuring the reader:

- removed the Testing Configuration "PPS\_MC\_Refund".

- added the Testing Requirement "12 Refund"



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# 1 Introduction

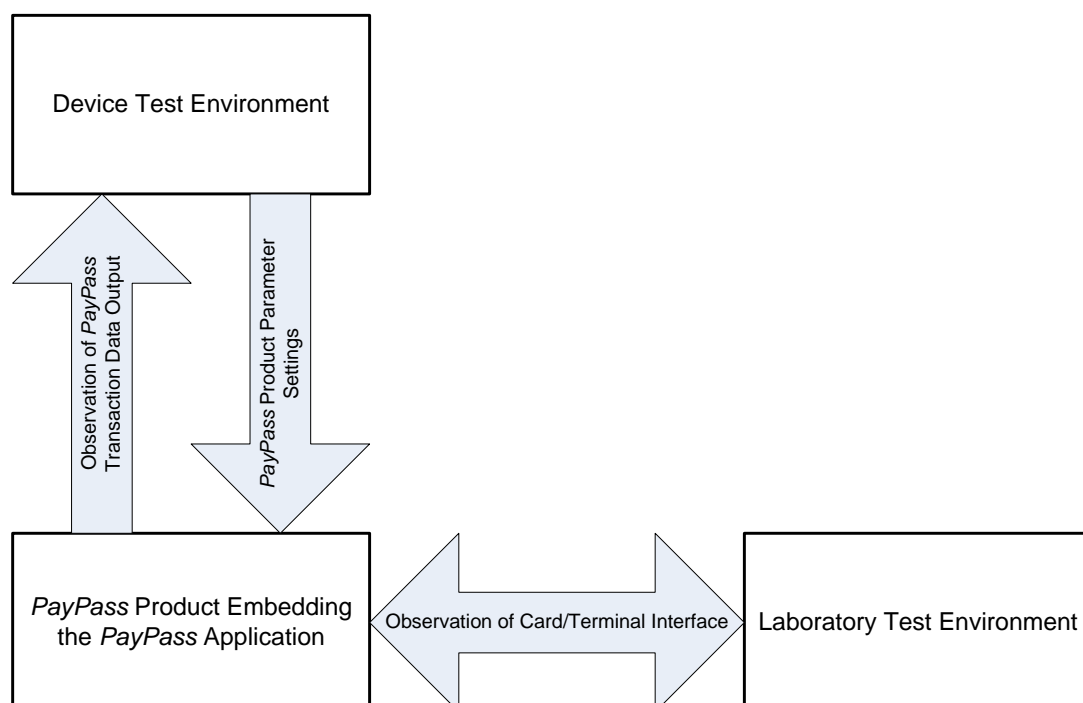
This chapter provides an introduction to the *PayPass* Testing Environment. (Terminal products)

## Purpose

MasterCard requires that *PayPass* Products implementing [*PayPass Mag Stripe Technical Specifications*] or [*PayPass M/Chip Technical Specifications*] and submitted for *PayPass* Type Approval Level 2 (*PayPass* TTA L2) are to be tested against the relevant specification.

To test the compliance of the *PayPass* Product implementation to the related *PayPass* technical specification(s), the *PayPass* Product has to be tested in a determined *PayPass* Testing Environment, as described in Figure 1-1 below and further detailed in this document.

**Figure 1-1: Schematic View of the *PayPass* Testing Environment**



The *PayPass* Testing Environment is composed of two parts:

- The Laboratory Test Environment provided by the Test Laboratory is constituted by the laboratory's test tools qualified by MasterCard. The Laboratory Test Environment allows the control and the observation of the interface between the *PayPass* Product and the card (tested protocol).

- The Device Test Environment allows the observation of the *PayPass* transaction data output and the configuration of the *Paypass* Product data and parameters. The Device Test Environment must be provided by the vendor at the same time as the *PayPass* Product Samples.

The purpose of this document is to describe the requirements of the *PayPass* Testing Environment. This document is structured as follows:

- Chapter 2: Laboratory Test Environment
- Chapter 3: Requirements for Device Test Environment.

## Audience

This document is intended for use by Vendors, that is, by manufacturers and suppliers of *PayPass* Products.

This document is aimed at the Program Manager or Project Manager responsible for the delivery of their *PayPass* Products through the *PayPass* Vendor Product Approval Process.

## Reader Guidance

This document describes the *PayPass* Testing Environment for *PayPass* Products supporting all types of *PayPass* applications.

Information specific to *PayPass* – Mag Stripe applications is indicated with the following symbol in the margin:

*pay***pass**<sup>™</sup>  
Mag Stripe

If you submit a *PayPass* Product supporting only *PayPass* – Mag Stripe application for approval, you can skip the information specific to *PayPass* – M/Chip products.

Information specific to *PayPass* – M/Chip applications is indicated with the following symbol in the margin:

*pay***pass**<sup>™</sup>  
M/Chip

## Related Information

The following reference materials may be of use to the reader of this document.

**NOTE:**

**MasterCard reserves the right to release updates to these documents and any documents it references. Vendors must therefore check for the latest documentation versions and the impact of any amendments they contain before starting the vendor testing process.**

**EMV Contactless Protocol**

EMV Contactless Communication Protocol Specification 2.0



**PayPass Mag Stripe Technical Specifications**

*PayPass* – Mag Stripe Technical Specifications



**PayPass M/Chip Technical Specifications**

*PayPass* - M/Chip Reader Card Application Interface Specification

## Acronyms

The following acronyms are used in this document:

Acronym	Description
EMV	Europay MasterCard Visa
TTA L1	Terminal Type Approval Level 1
TTA L2	Terminal Type Approval Level 2

## Terminology

This section explains the terms used in this specification.

**Contactless Card Reader** – Product integrating a PCD, to be connected to a Terminal, to allow the Terminal to perform the financial transaction. A Contactless Card Reader may also include other components such as PED, *PayPass* Application, contact interface module, printer.

**Fully Integrated Terminal** – A *PayPass* Product integrating a PCD and the *PayPass* Application and which can process a Payment transaction without needing to be connected to a Contactless Card Reader. It may also include other components and interfaces such as PIN Entry Devices (PED), printer or host communications.

**Intelligent Contactless Card Reader** – A Contactless Card Reader which also integrates a *PayPass* Application.

**Operational Terminal** – Any terminal hardware/software not part of the submitted product that enables terminal functionality, i.e. hardware into which a submitted product must be integrated to form a payment/service providing system e.g. vending machine.

**PayPass Application** – The software module residing on a *PayPass* Product and which implements the [*PayPass Mag Stripe Technical Specifications*] or the [*PayPass M/Chip Technical Specifications*].

**PayPass Product** – A product or combination of products incorporating at least a PCD or a *PayPass* Application. Only *PayPass* Products integrating a PCD and a *PayPass* Application and a PED, if available on that *PayPass* Product, will be approved by MasterCard.

**PayPass Product Component** – Component whose assessment is relevant for *PayPass* Product Approval. There are three *PayPass* Product Components: the PCD, the *PayPass* Application and the PIN Entry Device (if any).

**PayPass Terminal** – A Fully Integrated Terminal or the combination of a Contactless Card Reader and a terminal covering the *PayPass* Application.

**Proximity Coupling Device (PCD)** – A product component constituted of a combination of hardware and software and which implements [*EMV Contactless Protocol*]. The PCD uses inductive coupling to provide power to the PICC and also controls the data exchange with the PICC, up to and including the transport layer.

**Sample** – A *PayPass* Product picked out of production for testing.

**Transparent Contactless Card Reader** – A Contactless Card Reader that does not integrate the *PayPass* Application..

## 2 Laboratory Test Environment Description

pay **pass**<sup>™</sup>  
Mag Stripe

pay **pass**<sup>™</sup>  
M/Chip

The card probe test application simulates different card profiles to check whether the submitted *PayPass* Product supports all the mandatory features of:

- For *PayPass*-Mag Stripe: [*PayPass Mag Stripe Technical Specifications*].
- For *PayPass*-M/Chip: [*PayPass M/Chip Technical Specifications*].

TTA L2, as performed by a Test Laboratory, includes tests with *PayPass* ETEC cards. This enhances interoperability and increases the confidence that the *PayPass* Product will function correctly during integration and network testing.

MasterCard ETEC test cards for TTA L2 testing can be obtained by contacting: [test\\_tools@fime.com](mailto:test_tools@fime.com).



## 3 Requirements for Device Test Environment

Ideally, the Device Test Environment for TTA L2 is integrated in a single environment, running on a PC (Personal Computer).

### Observation of *PayPass* Transaction Data Output

The Device Test Environment must provide access to:

- **PayPass Mag Stripe data output**, as provided by the reader at the end of the transaction.
- **PayPass M/Chip data output**, as provided by the reader at the end of the transaction.



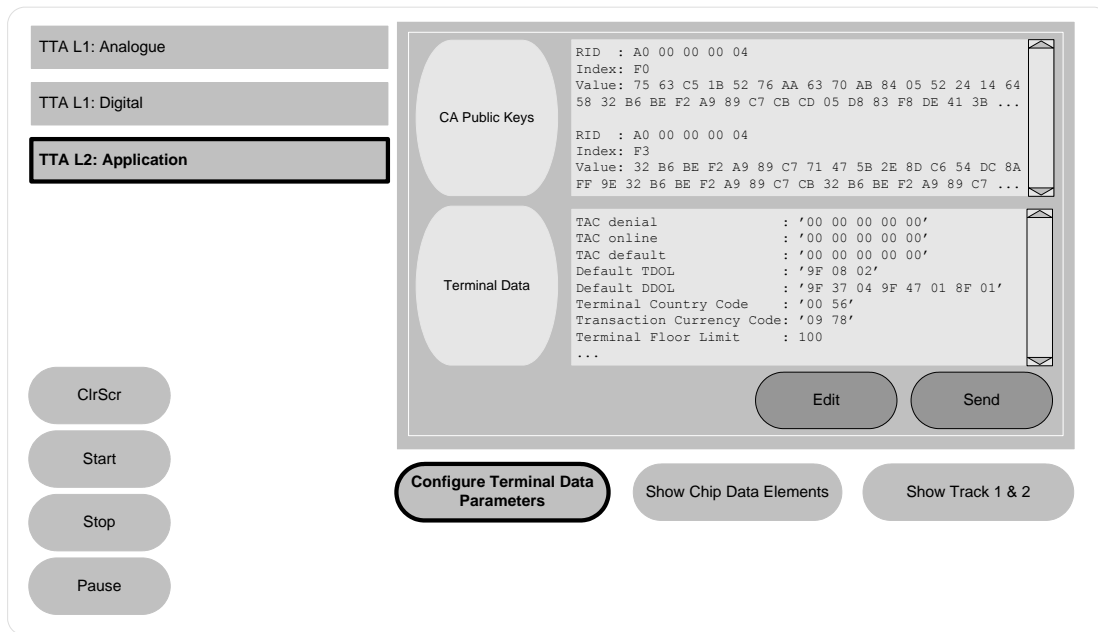
The Testing Environment must comply to the requirements defined in *[PayPass Mag Stripe Technical Specifications]* and the *[PayPass M/Chip Technical Specifications]* section “Completion” and to the requirements defined in this document in section “Application Testing Requirements”

## PayPass Product Parameter Settings

The Testing Environment must also provide means to configure *PayPass* Product data and parameters. See example in Figure 3-1 below.



**Figure 3-1: PC Interface for *PayPass* Product Configuration Modification**



### TTA L2 – Application Testing Requirements

For testing the *PayPass* Application, the submitted *PayPass* Product must be configured as indicated below.

1. List of AIDs The submitted *PayPass* Product must contain the list of AIDs listed in Table 3-1.

**Table 3-1: List of AIDs**

Application Name	AID
MasterCard	A0 00 00 00 04 10 10
Maestro	A0 00 00 00 04 30 60
TEST	B0 12 34 56 78

2. Kernel linkage The MasterCard, Maestro and Test AIDs must be linked to the *PayPass* kernel and shall therefore be able to complete a transaction (i.e. support [*PayPass Mag Stripe Technical Specifications*] or [*PayPass M/Chip Technical Specifications*], as appropriate).
3. Mono-appli If the submitted *PayPass* Product is tested as a multi-application terminal, this does not prevent the submitted *PayPass* Product from supporting only one AID when deployed in the field.
4. Data Record If the transaction completed successfully then the Device Test Environment must indicate the Data Record details as listed in the specifications.  
  
When displayed, Track 1 must appear in ASCII notation. Other data elements must appear in hexadecimal notation.
5. Cut & paste If the transaction was completed successfully, means must be provided so that the chip data elements and/or the Track 1 and Track 2 data can be cut & paste into a document (e.g. using CTRL C on screen capture).
6. Start The Testing Environment must have a specific option/function that allows new transactions to be started even if the card remains on the submitted *PayPass* Product. Note that if this option/function is not activated, the submitted *PayPass* Product must implement the removal sequence as described in section 9.5 of [*EMV Contactless Protocol*].



The following Device Testing Environment requirements apply to *PayPass*-Mag Stripe products only:

7. Direct Selection When the submitted *PayPass* Product supports *PayPass* MagStripe only then it may support the “Direct Selection” feature as stated in the “Note” at the end of [*PayPass Mag Stripe Technical Specifications*] section “1 Application Selection”. If so, the submitted *PayPass* Product shall also support the PPSE and the AID configurations defined above for the testing needs. The Device Test Environment shall permit to deactivate the PPSE and activate the Direct Selection. When the “Direct Selection” mode is activated the Device Testing Environment shall permit to choose the application to be loaded among the ones listed in “List of AIDs” above.
8. Transaction result The Device Test Environment must be able to indicate the transaction result.

## Requirements for Device Test Environment

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The following Device Testing Environment requirements apply to *PayPass-M/Chip* Products only:

9. Proprietary Selection According to *[PayPass M/Chip Technical Specifications]* section “3.4 Application Selection” the submitted product may support a proprietary application selection method. It is recommended to not deactivate this proprietary method during the test session. The information below list the assumptions made during the Level 2 test implementation and detail how the Level 2 tests will treat the proprietary selection method. If the vendor feels that the submitted product will not meet these assumptions and therefore could be unable to run the Level2 tests then he must contact [testing\\_terminal@paypass.com](mailto:testing_terminal@paypass.com).

### **Level 2 assumptions about proprietary application selection method (if any):**

According to *[PayPass M/Chip Technical Specifications]* section “3.4 Application Selection” the proprietary method may occur prior or after PPSE is sent.

#### **1. Level2 test implementation prior to PPSE:**

Prior to PPSE the Level2 tests will make the following checks:

Do While the received command is a PPSE or reader aborts:

- If the command received is a Select with an AID different from the AIDs listed in “List of AIDs” above then the card simulator will return ‘6A82’
- If the command received is a Select PSE then the card simulator will return ‘6A82’
- If the command received is a Select PPSE then the test will start (card simulator will return PPSE response etc...)
- If the command received is any other command then the card simulator will return ‘6A81’

Loop [get next command APDU]

Also, when the reader supports a proprietary selection method prior to the PPSE it will certainly not wait for the end of the Pre-Processing to Power up the contactless interface. Therefore the Level 2 tests will not check the requirement stated in *[PayPass M/Chip Technical Specifications]* section 3.3.1.1.

#### **2. Level2 test implementation after PPSE:**

When the candidate list is empty or when the card returns status bytes other than ‘9000’ to the Select PPSE command the submitted PayPass Product may

switch to a proprietary selection method. In this case the relating requirement (*PayPass M/Chip Technical Specifications* section 3.4.2.1) will not be tested.

10. Transaction CVM      The Device Test Environment must be able to indicate the outcome of the CVM Selection function. Possible values are 'No CVM', 'Signature', 'Online PIN'.  
  
In case of a Fully Intergrated Terminal, a printed ticket could identify the transaction CVM 'Signature', an Online PIN request could identify the transaction CVM 'OnlinePIN'. Neither printed ticket nor PIN request could identify a 'No CVM' CVM outcome.
11. Transaction Outcome      The Device Test Environment must be able to indicate the Transaction Outcome values listed in the specifications (see Data Objects Dictionary page 69).  
  
In case the values are not the same as the one defined in the specifications ("Approved", "declined", ...) then the vendor shall detail how to identify the 5 values.
12. Refund      The reader must be able to trigger a Refund transaction, if supported. (Transaction Type: '20')
13. Host simulator      In case the submitted *PayPass* Product manages a communication with the host (typically the case of fully integrated readers) then a host simulator shall be provided in order to return at least the following response codes (ARC):
  - '30 30' (Approved),
  - '30 31' (Call your bank),
  - '30 32' (not specific),
  - '35 31' (decline),
  - '50 50' (not specific)
14. ODC      In case the submitted *PayPass* Product supports Online Data Capture (only relevant for fully integrated *PayPass* readers) then the host simulator shall be able to return an incorrect response so the reader sends a reversal.
15. Data object configurat<sup>o</sup>      The data objects listed in *PayPass M/Chip Technical Specifications* sections 5.4.1.2, 5.4.1.3, 5.4.1.4 must be configurable.

## Requirements for Device Test Environment

16. Data object configurat<sup>o</sup> (5.4.1.2) Unless otherwise specified in the tests or in section *PayPass Product Testing Configurations*, the data objects listed in *[PayPass M/Chip Technical Specifications]* section 5.4.1.2 must have the values defined in Table 3-2 for the three AIDs listed above.

**Table 3-2: Data object configuration (5.4.1.2)**

Data Object Name	Test value
Additional Terminal Capabilities	As per the <i>PayPass</i> Product capabilities
Application Version Number	0002
Default UDOL (if applicable)	9F6A04
Mag Stripe Application Version Number (if applicable)	0001
Merchant Category Code	Any value different from zero
Merchant Custom Data	Any value different from zero
<i>PayPass</i> – Mag Stripe Indicator	<i>PayPass</i> – Mag Stripe is: “MasterCard” AID: allowed “Maestro” AID: NOT allowed “Test” AID: allowed
Terminal Action Codes	All zeroes
Terminal Type	As per the <i>PayPass</i> Product capabilities. It must be the same value for the three AIDs.
Terminal Capabilities – No CVM Required	Must be the same values as indicated in the ICS section "4.10 Terminal Data Element Values - Terminal Capabilities".
Terminal Capabilities – CVM Required	Must be the same values as indicated in the ICS section "4.10 Terminal Data Element Values - Terminal Capabilities".
Terminal Contactless Transaction Limit	300.00
Terminal Contactless Floor Limit	Offline/Online capable: 100.00 Offline-Only: maximum Online-Only: 0
Terminal CVM Required Limit	“MasterCard” AID: 10.00 “Maestro” AID: 300.00 “Test” AID: 10.00

17. Data object configuration<sup>o</sup> (5.4.1.3)      The CA Public Keys related data elements are defined in section CA Public Keys.
18. Data object configuration<sup>o</sup> (5.4.1.4)      Unless otherwise specified in the tests or in section *PayPass* Product Testing Configurations, the data objects listed in *[PayPass M/Chip Technical Specifications]*, section 5.4.1.4 must have the values defined in Table 3-3 for the three AIDs listed above.

**Table 3-3: Data object configuration (5.4.1.4)**

Data Object Name	Test value
Amount Authorized (Binary)	'0000 05DC' (15.00) This is the default transaction amount value to be used.
Amount Authorized (Numeric)	'000000 001500' (15.00) This is the default transaction amount value to be used.
Amount Other (Binary)	All zeroes
Amount Other (Numeric)	All zeroes
Transaction Category Code	Any value in line with the Merchant Category Code
Transaction Currency Code	0978 (euro)
Transaction Currency Exponent	2
Transaction Date	Current
Transaction Time	Current
Transaction Type	'00' (goods and services)

19. Exception list      If supported by the submitted *PayPass* Product, the exception list must include the following data:

PAN: 54 13 33 90 00 00 15 96

PAN sequence number: 00

## Requirements for Device Test Environment

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20. Revocation list      If supported by the submitted *PayPass* Product, the revocation list must include the data defined in Table 3-4.
- The laboratory must be able to add and remove an item from the Revocation list.

**Table 3-4: Revocation List data**

<b>RID: A0 00 00 00 04</b>	<b>RID: B0 12 34 56 78</b>
<b>CA PK Index: F8</b>	<b>CA PK Index: F8</b>
<b>Certificate Serial Number:</b>	<b>Certificate Serial Number:</b>
00 00 10	00 00 10
00 00 11	00 00 11
00 01 01	00 01 01
00 01 10	00 01 10
00 01 11	00 01 11
00 10 00	00 10 00
00 10 01	00 10 01
00 10 10	00 10 10
00 10 11	00 10 11
00 11 00	00 11 00
00 11 01	00 11 01
00 11 10	00 11 10
00 11 11	00 11 11
01 00 00	01 00 00
01 00 01	01 00 01
01 00 10	01 00 10
01 00 11	01 00 11
01 01 00	01 01 00
01 01 01	01 01 01
01 01 11	01 01 11
01 10 00	01 10 00
01 10 01	01 10 01
01 10 10	01 10 10
01 10 11	01 10 11
01 11 00	01 11 00
01 11 01	01 11 01
01 11 10	01 11 10
01 11 11	01 11 11
10 00 00	10 00 00
10 00 01	10 00 01

### PayPass Product Testing Configurations



The following Device Testing Environment requirements apply to *PayPass*–Mag Stripe Products only:

<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_MStripe1	The submitted <i>PayPass</i> Product follows the configuration requirement listed in section TTA L2 – Application Testing Requirements, and: Mag Stripe Application Version Number is ‘0001’.
PPS_MStripe2	If the submitted <i>PayPass</i> Product supports Direct Selection then: <ul style="list-style-type: none"> <li>– Direct Selection must be activated</li> <li>– the configured AID must be: ‘A0 00 00 00 04 10 10’ (MasterCard)</li> </ul> The rest is as per configuration PPS_MStripe1.

## Requirements for Device Test Environment

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The following Device Testing Environment requirements apply to *PayPass*–M/Chip Products only:

**NOTE:**

**According to [PayPass M/Chip Technical Specifications] section 5.4.1.2, some features listed below should in theory be duplicated for MasterCard and Maestro AIDs.**

**For example, supporting different “Additional Terminal Capabilities” could lead to several supported “Character sets”.**

**In order to ease the Level 2 testing and unless otherwise specified in this document, the features listed below are assumed to be the same for all AIDs supported. If it is not the case, that is, if the vendor really wants some features listed below to be separate for each AID then this shall be treated as a change to the *PayPass* Product and regression tests will be required for the additional configuration(s).**

<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_MChip1	The submitted <i>PayPass</i> Product follows the configuration requirement listed in section TTA L2 – Application Testing Requirements, and: Terminal Country Code: 00 56
PPS_MChip2	Same as PPS_MChip1 except for: TAC online = 7C D8 FC F8 F0 (MasterCard AID TAC)
PPS_MChip3	Same as PPS_MChip1 except for: TAC denial = 7C D8 FC F8 F0 (MasterCard AID TAC)
PPS_MChip4	Same as PPS_MChip1 except for: TAC online = 00 20 00 00 00 (MasterCard AID TAC)
PPS_MChip5	Same as PPS_MChip1 except for: TAC denial = 00 20 00 00 00 (MasterCard AID TAC)
PPS_MChip6	Same as PPS_MChip1 except for: TAC default = 00 40 00 00 00 (MasterCard AID TAC)
PPS_VisualTest	Same as PPS_Mchip1 but no executable test (Visual check test)

## Requirements for Device Test Environment

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<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_TIP	<p>Same as PPS_Mchip1 except for TACs. TACs must have the same values for all AIDs.</p> <p>Case of Online capable readers:            TAC denial: 00 00 00 00 00            TAC online: FC 50 8C 88 00            TAC default: FC 50 8C 88 00</p> <p>Case of Offline-Only readers:            TAC denial: FC 50 80 88 00            TAC online: 00 00 00 00 00            TAC default: 00 00 00 00 00</p> <p>Maestro Terminal Capabilities indicate "SDA not supported".</p> <p>MasterCard Terminal Capabilities remain unchanged.</p>
PPS_perf	<p>Specific configuration is required during the <i>PayPass</i> performance tests. This is detailed in the relating specifications "<i>PayPass – Performance Measurement, Version 1.3 - January 2008</i>".</p>

<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_Select1	<p>Same as PPS_MChip1 except for:</p> <ol style="list-style-type: none"> <li>1. MasterCard: A0 00 00 00 04 10 10            Terminal Contactless Transaction Limit = 20.00            Terminal Contactless floor limit = 100.00            Terminal CVM Required Limit = 51.50</li> <li>2. Maestro: A0 00 00 00 04 30 60            Terminal Contactless Transaction Limit = 400.00            Terminal contactless floor limit = 200.00            Terminal CVM Required Limit = 75.00</li> <li>3. TEST: B0 12 34 56 78            Terminal Contactless Transaction Limit = 500.00            Terminal contactless floor limit = 150.00            Terminal CVM Required Limit = 102.50</li> </ol>

## Requirements for Device Test Environment

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<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_Select2	<p>Same as PPS_MChip1 except for:</p> <ol style="list-style-type: none"> <li>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 7000.00 Terminal Contactless Floor Limit = 5000.00 Terminal CVM Required Limit = 6030.00</li> <li>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 6000.00 Terminal Contactless Floor Limit = 9.00 Terminal CVM Required Limit = 6000.00</li> <li>3. TEST: B0 12 34 56 78 - No specific value.</li> </ol>
PPS_Select3	<p>Same as PPS_MChip1 except for:</p> <ol style="list-style-type: none"> <li>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 2600.00 Terminal Contactless Floor Limit = 100.00 Terminal CVM Required Limit = 51.50</li> <li>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 2600.00 Terminal Contactless Floor Limit = 200.00 Terminal CVM Required Limit = 102.50</li> <li>3. TEST: B0 12 34 56 78 - No specific value.</li> </ol>

## Requirements for Device Test Environment

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<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_Select4	<p>Same as PPS_MChip1 except for:</p> <p>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 300.00 Terminal CVM Required Limit = 300.00 Terminal Contactless floor limit = 300.00</p> <p>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 300.00 Terminal CVM Required Limit = 300.00 Terminal contactless floor limit = 300.00</p> <p>3. Test: B0 12 34 56 78 Terminal Contactless Transaction Limit = 1000.00 Terminal CVM Required Limit = 1000.00 Terminal contactless floor limit = 1000.00</p>
PPS_Select5	<p>Same as PPS_MChip1 except for:</p> <p>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 100.00 Terminal Contactless floor limit = 150.00</p> <p>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 120.00 Terminal contactless floor limit = 100.00</p> <p>3. Test: B0 12 34 56 78 Terminal Contactless Transaction Limit = 100 Terminal CVM Required Limit = 100 Terminal contactless floor limit = 100</p>

## Requirements for Device Test Environment

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<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_Select6	<p>Same as PPS_MChip1 except for:</p> <ol style="list-style-type: none"> <li>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 100.00 Terminal Contactless floor limit = 200.00</li> <li>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 100.00 Terminal contactless floor limit = 200.00</li> <li>3. Test: B0 12 34 56 78 Terminal Contactless Transaction Limit = 1000.00 Terminal CVM Required Limit = 900.00 Terminal contactless floor limit = 1000.00</li> </ol>
PPS_Select7	<p>Same as PPS_MChip1 except for:</p> <ol style="list-style-type: none"> <li>1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 200.00 Terminal Contactless floor limit = 100.00</li> <li>2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 200.00 Terminal CVM Required Limit = 200.00 Terminal contactless floor limit = 100.00</li> <li>3. Test: B0 12 34 56 78 Terminal Contactless Transaction Limit = 1000.00 Terminal CVM Required Limit = 1000.00 Terminal contactless floor limit = 900.00</li> </ol>

## Requirements for Device Test Environment

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<b>PayPass Product Configuration</b>	<b>Description</b>
PPS_Select8	Same as PPS_MChip1 except for: 1. MasterCard: A0 00 00 00 04 10 10 Terminal Contactless Transaction Limit = 300.00 Terminal CVM Required Limit = 200.00 Terminal Contactless floor limit = 200.00  2. Maestro: A0 00 00 00 04 30 60 Terminal Contactless Transaction Limit = 300.00 Terminal CVM Required Limit = 200.00 Terminal contactless floor limit = 200.00  3. Test: B0 12 34 56 78 Terminal Contactless Transaction Limit = 1000.00 Terminal CVM Required Limit = 900.00 Terminal contactless floor limit = 900.00

# Requirements for Device Test Environment

## CA Public Keys



This section applies to *PayPass*-M/Chip Products only.

The following table lists the CA Public Keys used for testing, in case the *PayPass* reader supports offline data authentication.

The Checksum is calculated as follow: SHA(RID + Index + Modulus + Exp)

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
0	A0 00 00 00 04	00	9C 6B E5 AD B1 0B 4B E3 DC E2 09 9B 4B 21 06 72	160	3	EC 0A 59	EVAL
			B8 96 56 EB A0 91 20 4F 61 3E CC 62 3B ED C9 C6			D3 5D 19	
			D7 7B 66 0E 8B AE EA 7F 7C E3 0F 1B 15 38 79 A4			F0 31 E9	
			E3 64 59 34 3D 1F E4 7A CD BD 41 FC D7 10 03 0C			E8 CB EC	
			2B A1 D9 46 15 97 98 2C 6E 1B DD 08 55 4B 72 6F			56 DB 80	
			5E FF 79 13 CE 59 E7 9E 35 72 95 C3 21 E2 6D 0B			E2 2B 1D	
			8B E2 70 A9 44 23 45 C7 53 E2 AA 2A CF C9 D3 08			E1 30	
			50 60 2F E6 CA C0 0C 6D DF 6B 8D 9D 9B 48 79 B2				
			82 6B 04 2A 07 F0 E5 AE 52 6A 3D 3C 4D 22 C7 2B				
9E AA 52 EE D8 89 38 66 F8 66 38 7A C0 5A 13 99							
1	A0 00 00 00 04	02	A9 9A 6D 3E 07 18 89 ED 9E 3A 0C 39 1C 69 B0 B8	192	3	33 40 8B	EVAL
			04 FC 16 0B 2B 4B DD 57 0C 92 DD 5A 0F 45 F5 3E			96 C8 14	
			86 21 F7 C9 6C 40 22 42 66 73 5E 1E E1 B3 C0 62			74 2A D7	
			38 AE 35 04 63 20 FD 8E 81 F8 CE B3 F8 B4 C9 7B			35 36 C7	
			94 09 30 A3 AC 5E 79 00 86 DA D4 1A 6A 4F 51 17			2F 09 26	
			BA 1C E2 43 8A 51 AC 05 3E B0 02 AE D8 66 D2 C4			E4 47 1E	
			58 FD 73 35 90 21 A1 20 29 A0 C0 43 04 5C 11 66			8E 47	
			4F E0 21 9E C6 3C 10 BF 21 55 BB 27 84 60 9A 10				
			64 21 D4 51 63 79 97 38 C1 C3 09 09 BB 6C 6F E5				
2B BB 76 39 7B 97 40 CE 06 4A 61 3F F8 41 11 85							
F0 88 42 A4 23 EA D2 0E DF FB FF 1C D6 C3 FE 0C							
98 21 47 91 99 C2 6D 85 72 CC 8A FF F0 87 A9 C3							
2	A0 00 00 00 04	05	A1 F5 E1 C9 BD 86 50 BD 43 AB 6E E5 6B 89 1E F7	128	3	53 D0 49	EVAL
			45 9C 0A 24 FA 84 F9 12 7D 1A 6C 79 D4 93 0F 6D			03 B4 96	
			B1 85 2E 25 10 F1 8B 61 CD 35 4D B8 3A 35 6B D1			F5 95 44	
			90 B8 8A B8 DF 04 28 4D 02 A4 20 4A 7B 6C B7 C5			A8 43 09	
			55 19 77 A9 B3 63 79 CA 3D E1 A0 8E 69 F3 01 C9			AF 16 92	
			5C C1 C2 05 06 95 92 75 F4 17 23 DD 5D 29 25 29			51 F2 89	
			05 79 E5 A9 5B 0D F6 32 3F C8 E9 27 3D 6F 84 91			68 74	
			98 C4 99 62 09 16 6D 9B FC 97 3C 36 1C C8 26 E1				

## Requirements for Device Test Environment

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing		
3	A0 00 00 00 04	EF	A1 91 CB 87 47 3F 29 34 9B 5D 60 A8 8B 3E AE E0	248	3	21 76 6E	ETEC		
			97 3A A6 F1 A0 82 F3 58 D8 49 FD DF F9 C0 91 F8					BB 0E E1	
			99 ED A9 79 2C AF 09 EF 28 F5 D2 24 04 B8 8A 22					22 AF B6	
			93 EE BB C1 94 9C 43 BE A4 D6 0C FD 87 9A 15 39					5D 78 45	
			54 4E 09 E0 F0 9F 60 F0 65 B2 BF 2A 13 EC C7 05					B7 3D B4	
			F3 D4 68 B9 D3 3A E7 7A D9 D3 F1 9C A4 0F 23 DC					6B AB 65	
			F5 EB 7C 04 DC 8F 69 EB A5 65 B1 EB CB 46 86 CD					42 7A°	
			27 47 85 53 0F F6 F6 E9 EE 43 AA 43 FD B0 2C E0						
			0D AE C1 5C 7B 8F D6 A9 B3 94 BA BA 41 9D 3F 6D						
			C8 5E 16 56 9B E8 E7 69 89 68 8E FE A2 DF 22 FF						
			7D 35 C0 43 33 8D EA A9 82 A0 2B 86 6D E5 32 85						
			19 EB BC D6 F0 3C DD 68 66 73 84 7F 84 DB 65 1A						
			B8 6C 28 CF 14 62 56 2C 57 7B 85 35 64 A2 90 C8						
			55 6D 81 85 31 26 8D 25 CC 98 A4 CC 6A 0B DF FF						
			DA 2D CC A3 A9 4C 99 85 59 E3 07 FD DF 91 50 06						
			D9 A9 87 B0 7D DA EB 3B						
			4					A0 00 00 00 04	F1
29 4A AB BB 82 8C 5A 83 4D 73 AA E2 7C 99 B0 B0	A1 67 AB	EVAL							
53 A9 02 78 00 72 39 B6 45 9F F0 BB CD 7B 4B 9C	5A 85 D8								
6C 50 AC 02 CE 91 36 8D A1 BD 21 AA EA DB C6 53	C3 D5 5E								
47 33 7D 89 B6 8F 5C 99 A0 9D 05 BE 02 DD 1F 8C	CB 9B 05								
5B A2 0E 2F 13 FB 2A 27 C4 1D 3F 85 CA D5 CF 66	17 A1 A5								
68 E7 58 51 EC 66 ED BF 98 85 1F D4 E4 2C 44 C1	B4 BB								
D5 9F 59 84 70 3B 27 D5 B9 F2 1B 8F A0 D9 32 79									
FB BF 69 E0 90 64 29 09 C9 EA 27 F8 98 95 95 41									
AA 67 57 F5 F6 24 10 4F 6E 1D 3A 95 32 F2 A6 E5									
15 15 AE AD 1B 43 B3 D7 83 50 88 A2 FA FA 7B E7									
5	A0 00 00 00 04	F3	98 F0 C7 70 F2 38 64 C2 E7 66 DF 02 D1 E8 33 DF	144	3	A6 9A C7	EVAL		
			F4 FF E9 2D 69 6E 16 42 F0 A8 8C 56 94 C6 47 9D					60 3D AF	
			16 DB 15 37 BF E2 9E 4F DC 6E 6E 8A FD 1B 0E B7					56 6E 97	
			EA 01 24 72 3C 33 31 79 BF 19 E9 3F 10 65 8B 2F					2D ED C2	
			77 6E 82 9E 87 DA ED A9 C9 4A 8B 33 82 19 9A 35					CB 43 3E	
			0C 07 79 77 C9 7A FF 08 FD 11 31 0A C9 50 A7 2C					07 E8 B0	
			3C A5 00 2E F5 13 FC CC 28 6E 64 6E 3C 53 87 53					1A 9A°	
			5D 50 95 14 B3 B3 26 E1 23 4F 9C B4 8C 36 DD D4						
4B 41 6D 23 65 40 34 A6 6F 40 3B A5 11 C5 EF A3									

# Requirements for Device Test Environment

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
6	A0	F5	A6 E6 FB 72 17 95 06 F8 60 CC CA 8C 27 F9 9C EC	248	65537	C2 23 98	EVAL
	00		D9 4C 7D 4F 31 91 D3 03 BB EE 37 48 1C 7A A1 5F			04 C8 09	
	00		23 3B A7 55 E9 E4 37 63 45 A9 A6 7E 79 94 BD C1			81 70 BE	
	00		C6 80 BB 35 22 D8 C9 3E B0 CC C9 1A D3 1A D4 50			52 D6 D5	
	04		DA 30 D3 37 66 2D 19 AC 03 E2 B4 EF 5F 6E C1 82			D4 15 9E	
			82 D4 91 E1 97 67 D7 B2 45 42 DF DE FF 6F 62 18			81 CE 84	
			55 03 53 20 69 BB B3 69 E3 BB 9F B1 9A C6 F1 C3			66 BF	
			0B 97 D2 49 EE E7 64 E0 BA C9 7F 25 C8 73 D9 73				
			95 3E 51 53 A4 20 64 BB FA BF D0 6A 4B B4 86 86				
			0B F6 63 74 06 C9 FC 36 81 3A 4A 75 F7 5C 31 CC				
			A9 F6 9F 8D E5 9A DE CE F6 BD E7 E0 78 00 FC BE				
			03 5D 31 76 AF 84 73 E2 3E 9A A3 DF EE 22 11 96				
			D1 14 83 02 67 7C 72 0C FE 25 44 A0 3D B5 53 E7				
			F1 B8 42 7B A1 CC 72 B0 F2 9B 12 DF EF 4C 08 1D				
			07 6D 35 3E 71 88 0A AD FF 38 63 52 AF 0A B7 B2				
			8E D4 9E 1E 67 2D 11 F9				
7	A0	F6	A2 5A 6B D7 83 A5 EF 6B 8F B6 F8 30 55 C2 60 F5	224	3	50 29 09	EVAL
	00		F9 9E A1 66 78 F3 B9 05 3E 0F 64 98 E8 2C 3F 5D			ED 54 5E	
	00		1E 8C 38 F1 35 88 01 7E 2B 12 B3 D8 FF 6F 50 16			3C 8D BD	
	00		7F 46 44 29 10 72 9E 9E 4D 1B 37 39 E5 06 7C 0A			00 EA 58	
	04		C7 A1 F4 48 7E 35 F6 75 BC 16 E2 33 31 51 65 CB			2D 06 17	
			14 2B FD B2 5E 30 1A 63 2A 54 A3 37 1E BA B6 57			FE E9 F6	
			2D EE BA F3 70 F3 37 F0 57 EE 73 B4 AE 46 D1 A8			F6 84	
			BC 4D A8 53 EC 3C C1 2C 8C BC 2D A1 83 22 D6 85				
			30 C7 0B 22 BD AC 35 1D D3 60 68 AE 32 1E 11 AB				
			F2 64 F4 D3 56 9B B7 12 14 54 50 05 55 8D E2 60				
			83 C7 35 DB 77 63 68 17 2F E8 C2 F5 C8 5E 8B 5B				
			89 0C C6 82 91 1D 2D E7 1F A6 26 B8 81 7F CC C0				
			89 22 B7 03 86 9F 3B AE AC 14 59 D7 7C D8 53 76				
			BC 36 18 2F 42 38 31 4D 6C 42 12 FB DD 7F 23 D3				
8	A0	F7	94 EA 62 F6 D5 83 20 E3 54 C0 22 AD DC F0 55 9D	128	65537	EE B0 DD	EVAL
	00		8C F2 06 CD 92 E8 69 56 49 05 CE 21 D7 20 F9 71			9B 24 77	
	00		B7 AE A3 74 83 0E BE 17 57 11 5A 85 E0 88 D4 1C			BE E3 20	
	00		6B 77 CF 5E C8 21 F3 0B 1D 89 04 17 BF 2F A3 1E			9A 91 4C	
	04		59 08 DE D5 FA 67 7F 8C 7B 18 4A D0 90 28 FD DE			DB A9 4C	
			96 B6 A6 10 98 50 AA 80 01 75 EA BC DB BB 68 4A			1C 4A 9B	
			96 C2 EB 63 79 DF EA 08 D3 2F E2 33 1F E1 03 23			DE D9	
			3A D5 8D CD B1 E6 E0 77 CB 9F 24 EA EC 5C 25 AF				

## Requirements for Device Test Environment

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
9	A0	F8	A1 F5 E1 C9 BD 86 50 BD 43 AB 6E E5 6B 89 1E F7	128	3	F0 6E CC	EVAL
	00		45 9C 0A 24 FA 84 F9 12 7D 1A 6C 79 D4 93 0F 6D			6D 2A AE	
	00		B1 85 2E 25 10 F1 8B 61 CD 35 4D B8 3A 35 6B D1			BF 25 9B	
	00		90 B8 8A B8 DF 04 28 4D 02 A4 20 4A 7B 6C B7 C5			7E 75 5A	
	04		55 19 77 A9 B3 63 79 CA 3D E1 A0 8E 69 F3 01 C9			38 D9 A9	
			5C C1 C2 05 06 95 92 75 F4 17 23 DD 5D 29 25 29			B2 4E 2F	
			05 79 E5 A9 5B 0D F6 32 3F C8 E9 27 3D 6F 84 91			F3 DD	
			98 C4 99 62 09 16 6D 9B FC 97 3C 36 1C C8 26 E1				
10	A0	F9	A9 9A 6D 3E 07 18 89 ED 9E 3A 0C 39 1C 69 B0 B8	192	3	33 67 12	EVAL
	00		04 FC 16 0B 2B 4B DD 57 0C 92 DD 5A 0F 45 F5 3E			DC C2 85	
	00		86 21 F7 C9 6C 40 22 42 66 73 5E 1E E1 B3 C0 62			54 80 9C	
	00		38 AE 35 04 63 20 FD 8E 81 F8 CE B3 F8 B4 C9 7B			6A A9 B0	
	04		94 09 30 A3 AC 5E 79 00 86 DA D4 1A 6A 4F 51 17			23 58 DE	
			BA 1C E2 43 8A 51 AC 05 3E B0 02 AE D8 66 D2 C4			6F 75 51	
			58 FD 73 35 90 21 A1 20 29 A0 C0 43 04 5C 11 66			64 DB	
			4F E0 21 9E C6 3C 10 BF 21 55 BB 27 84 60 9A 10				
			64 21 D4 51 63 79 97 38 C1 C3 09 09 BB 6C 6F E5				
			2B BB 76 39 7B 97 40 CE 06 4A 61 3F F8 41 11 85				
			F0 88 42 A4 23 EA D2 0E DF FB FF 1C D6 C3 FE 0C				
			98 21 47 91 99 C2 6D 85 72 CC 8A FF F0 87 A9 C3				
11	A0	FA	A9 0F CD 55 AA 2D 5D 99 63 E3 5E D0 F4 40 17 76	144	3	5B ED 40	ETEC
	00		99 83 2F 49 C6 BA B1 5C DA E5 79 4B E9 3F 93 4D			68 D9 6E	
	00		44 62 D5 D1 27 62 E4 8C 38 BA 83 D8 44 5D EA A7			A1 6D 2D	
	00		41 95 A3 01 A1 02 B2 F1 14 EA DA 0D 18 0E E5 E7			77 E0 3D	
	04		A5 C7 3E 0C 4E 11 F6 7A 43 DD AB 5D 55 68 3B 14			60 36 FC	
			74 CC 06 27 F4 4B 8D 30 88 A4 92 FF AA DA D4 F4			7A 16 0E	
			24 22 D0 E7 01 35 36 C3 C4 9A D3 D0 FA E9 64 59			A9 9C	
			B0 F6 B1 B6 05 65 38 A3 D6 D4 46 40 F9 44 67 B1				
			08 86 7D EC 40 FA AE CD 74 0C 00 E2 B7 A8 85 2D				
12	B0	00	9C 6B E5 AD B1 0B 4B E3 DC E2 09 9B 4B 21 06 72	160	3	5D 29 70	EVAL
	12		B8 96 56 EB A0 91 20 4F 61 3E CC 62 3B ED C9 C6			E6 46 75	
	34		D7 7B 66 0E 8B AE EA 7F 7C E3 0F 1B 15 38 79 A4			72 7E 60	
	56		E3 64 59 34 3D 1F E4 7A CD BD 41 FC D7 10 03 0C			46 07 65	
	78		2B A1 D9 46 15 97 98 2C 6E 1B DD 08 55 4B 72 6F			A8 DB 75	
			5E FF 79 13 CE 59 E7 9E 35 72 95 C3 21 E2 6D 0B			34 2A E1	
			8B E2 70 A9 44 23 45 C7 53 E2 AA 2A CF C9 D3 08			47 83	
			50 60 2F E6 CA C0 0C 6D DF 6B 8D 9D 9B 48 79 B2				
			82 6B 04 2A 07 F0 E5 AE 52 6A 3D 3C 4D 22 C7 2B				
			9E AA 52 EE D8 89 38 66 F8 66 38 7A C0 5A 13 99				

# Requirements for Device Test Environment

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
13	B0	02	A9 9A 6D 3E 07 18 89 ED 9E 3A 0C 39 1C 69 B0 B8	192	3	29 4B E2	EVAL
	12		04 FC 16 0B 2B 4B DD 57 0C 92 DD 5A 0F 45 F5 3E			02 39 AB	
	34		86 21 F7 C9 6C 40 22 42 66 73 5E 1E E1 B3 C0 62			15 24 5A	
	56		38 AE 35 04 63 20 FD 8E 81 F8 CE B3 F8 B4 C9 7B			63 BE A4	
	78		94 09 30 A3 AC 5E 79 00 86 DA D4 1A 6A 4F 51 17			6C C6 C1	
			BA 1C E2 43 8A 51 AC 05 3E B0 02 AE D8 66 D2 C4			75 A2 55	
			58 FD 73 35 90 21 A1 20 29 A0 C0 43 04 5C 11 66			62 D1	
			4F E0 21 9E C6 3C 10 BF 21 55 BB 27 84 60 9A 10				
			64 21 D4 51 63 79 97 38 C1 C3 09 09 BB 6C 6F E5				
			2B BB 76 39 7B 97 40 CE 06 4A 61 3F F8 41 11 85				
			F0 88 42 A4 23 EA D2 0E DF FB FF 1C D6 C3 FE 0C				
			98 21 47 91 99 C2 6D 85 72 CC 8A FF F0 87 A9 C3				
14	B0	05	A1 F5 E1 C9 BD 86 50 BD 43 AB 6E E5 6B 89 1E F7	128	3	B9 A1 D6	EVAL
	12		45 9C 0A 24 FA 84 F9 12 7D 1A 6C 79 D4 93 0F 6D			5C AF E0	
	34		B1 85 2E 25 10 F1 8B 61 CD 35 4D B8 3A 35 6B D1			6B 05 4E	
	56		90 B8 8A B8 DF 04 28 4D 02 A4 20 4A 7B 6C B7 C5			DD 7E A8	
	78		55 19 77 A9 B3 63 79 CA 3D E1 A0 8E 69 F3 01 C9			25 97 AB	
			5C C1 C2 05 06 95 92 75 F4 17 23 DD 5D 29 25 29			85 F1 30	
			05 79 E5 A9 5B 0D F6 32 3F C8 E9 27 3D 6F 84 91			E6 63	
			98 C4 99 62 09 16 6D 9B FC 97 3C 36 1C C8 26 E1				
15	B0	F3	94 EA 62 F6 D5 83 20 E3 54 C0 22 AD DC F0 55 9D	128	65537	56 94 B0	EVAL
	12		8C F2 06 CD 92 E8 69 56 49 05 CE 21 D7 20 F9 71			D2 78 48	
	34		B7 AE A3 74 83 0E BE 17 57 11 5A 85 E0 88 D4 1C			18 14 A0	
	56		6B 77 CF 5E C8 21 F3 0B 1D 89 04 17 BF 2F A3 1E			5E 12 B5	
	78		59 08 DE D5 FA 67 7F 8C 7B 18 4A D0 90 28 FD DE			58 CE C1	
			96 B6 A6 10 98 50 AA 80 01 75 EA BC DB BB 68 4A			23 48 65	
			96 C2 EB 63 79 DF EA 08 D3 2F E2 33 1F E1 03 23			AA 5D	
			3A D5 8D CD B1 E6 E0 77 CB 9F 24 EA EC 5C 25 AF				
16	B0	F5	A2 5A 6B D7 83 A5 EF 6B 8F B6 F8 30 55 C2 60 F5	224	3	F7 5E 88	EVAL
	12		F9 9E A1 66 78 F3 B9 05 3E 0F 64 98 E8 2C 3F 5D			02 85 5C	
	34		1E 8C 38 F1 35 88 01 7E 2B 12 B3 D8 FF 6F 50 16			9B 14 02	
	56		7F 46 44 29 10 72 9E 9E 4D 1B 37 39 E5 06 7C 0A			7E 51 73	
	78		C7 A1 F4 48 7E 35 F6 75 BC 16 E2 33 31 51 65 CB			45 71 7E	
			14 2B FD B2 5E 30 1A 63 2A 54 A3 37 1E BA B6 57			5C 36 35	
			2D EE BA F3 70 F3 37 F0 57 EE 73 B4 AE 46 D1 A8			B9 1B	
			BC 4D A8 53 EC 3C C1 2C 8C BC 2D A1 83 22 D6 85				
			30 C7 0B 22 BD AC 35 1D D3 60 68 AE 32 1E 11 AB				
			F2 64 F4 D3 56 9B B7 12 14 54 50 05 55 8D E2 60				
			83 C7 35 DB 77 63 68 17 2F E8 C2 F5 C8 5E 8B 5B				
			89 0C C6 82 91 1D 2D E7 1F A6 26 B8 81 7F CC C0				
			89 22 B7 03 86 9F 3B AE AC 14 59 D7 7C D8 53 76				
			BC 36 18 2F 42 38 31 4D 6C 42 12 FB DD 7F 23 D3				

## Requirements for Device Test Environment

ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
17	B0	F6	A1 F5 E1 C9 BD 86 50 BD 43 AB 6E E5 6B 89 1E F7	128	3	E9 40 6B	EVAL
	12		45 9C 0A 24 FA 84 F9 12 7D 1A 6C 79 D4 93 0F 6D			65 10 C1	
	34		B1 85 2E 25 10 F1 8B 61 CD 35 4D B8 3A 35 6B D1			43 AB 1E	
	56		90 B8 8A B8 DF 04 28 4D 02 A4 20 4A 7B 6C B7 C5			9B 9D 79	
	78		55 19 77 A9 B3 63 79 CA 3D E1 A0 8E 69 F3 01 C9			A3 C1 DF	
			5C C1 C2 05 06 95 92 75 F4 17 23 DD 5D 29 25 29			F8 90 9A	
			05 79 E5 A9 5B 0D F6 32 3F C8 E9 27 3D 6F 84 91			34 7C	
			98 C4 99 62 09 16 6D 9B FC 97 3C 36 1C C8 26 E1				
18	B0	F7	98 F0 C7 70 F2 38 64 C2 E7 66 DF 02 D1 E8 33 DF	144	3	F7 81 13	EVAL
	12		F4 FF E9 2D 69 6E 16 42 F0 A8 8C 56 94 C6 47 9D			E8 60 F0	
	34		16 DB 15 37 BF E2 9E 4F DC 6E 6E 8A FD 1B 0E B7			30 A8 72	
	56		EA 01 24 72 3C 33 31 79 BF 19 E9 3F 10 65 8B 2F			92 3F CE	
	78		77 6E 82 9E 87 DA ED A9 C9 4A 8B 33 82 19 9A 35			93 E3 38	
			0C 07 79 77 C9 7A FF 08 FD 11 31 0A C9 50 A7 2C			1C 77 A4	
			3C A5 00 2E F5 13 FC CC 28 6E 64 6E 3C 53 87 53			2A 30	
			5D 50 95 14 B3 B3 26 E1 23 4F 9C B4 8C 36 DD D4				
			4B 41 6D 23 65 40 34 A6 6F 40 3B A5 11 C5 EF A3				
19	B0	F8	A9 9A 6D 3E 07 18 89 ED 9E 3A 0C 39 1C 69 B0 B8	192	3	66 46 9C	EVAL
	12		04 FC 16 0B 2B 4B DD 57 0C 92 DD 5A 0F 45 F5 3E			88 E7 DC	
	34		86 21 F7 C9 6C 40 22 42 66 73 5E 1E E1 B3 C0 62			11 15 29	
	56		38 AE 35 04 63 20 FD 8E 81 F8 CE B3 F8 B4 C9 7B			C7 D3 79	
	78		94 09 30 A3 AC 5E 79 00 86 DA D4 1A 6A 4F 51 17			D7 93 8C	
			BA 1C E2 43 8A 51 AC 05 3E B0 02 AE D8 66 D2 C4			8D F3 E4	
			58 FD 73 35 90 21 A1 20 29 A0 C0 43 04 5C 11 66			C2 5E	
			4F E0 21 9E C6 3C 10 BF 21 55 BB 27 84 60 9A 10				
			64 21 D4 51 63 79 97 38 C1 C3 09 09 BB 6C 6F E5				
			2B BB 76 39 7B 97 40 CE 06 4A 61 3F F8 41 11 85				
			F0 88 42 A4 23 EA D2 0E DF FB FF 1C D6 C3 FE 0C				
			98 21 47 91 99 C2 6D 85 72 CC 8A FF F0 87 A9 C3				

## Requirements for Device Test Environment

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ID	RID	Index	Modulus	Length	Exp	Check Sum	Testing
20	B0	F9	A6 E6 FB 72 17 95 06 F8 60 CC CA 8C 27 F9 9C EC	248	65537	AE AC A4	EVAL
	12		D9 4C 7D 4F 31 91 D3 03 BB EE 37 48 1C 7A A1 5F			54 80 C8	
	34		23 3B A7 55 E9 E4 37 63 45 A9 A6 7E 79 94 BD C1			83 4C B0	
	56		C6 80 BB 35 22 D8 C9 3E B0 CC C9 1A D3 1A D4 50			BE BD CC	
	78		DA 30 D3 37 66 2D 19 AC 03 E2 B4 EF 5F 6E C1 82			57 0B 7B	
			82 D4 91 E1 97 67 D7 B2 45 42 DF DE FF 6F 62 18			2B 74 BB	
			55 03 53 20 69 BB B3 69 E3 BB 9F B1 9A C6 F1 C3			4B 79	
			0B 97 D2 49 EE E7 64 E0 BA C9 7F 25 C8 73 D9 73				
			95 3E 51 53 A4 20 64 BB FA BF D0 6A 4B B4 86 86				
			0B F6 63 74 06 C9 FC 36 81 3A 4A 75 F7 5C 31 CC				
			A9 F6 9F 8D E5 9A DE CE F6 BD E7 E0 78 00 FC BE				
			03 5D 31 76 AF 84 73 E2 3E 9A A3 DF EE 22 11 96				
			D1 14 83 02 67 7C 72 0C FE 25 44 A0 3D B5 53 E7				
			F1 B8 42 7B A1 CC 72 B0 F2 9B 12 DF EF 4C 08 1D				
			07 6D 35 3E 71 88 0A AD FF 38 63 52 AF 0A B7 B2				
			8E D4 9E 1E 67 2D 11 F9				

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